SECTION FOUR : CIRCUIT DESCRIPTION

4.1 SIGNAL CIRCUITS

The following should be read in conjunction with BP2022 1650/6 Receiver Signal Circuits Block Diagram bound in Part 2. Refer to BP2021 1650/6 Chassis Interconnections & Misc. Modules for connections etc. between the modules described.

Circuit diagrams BP1968 RF & 1st. IF board and BP1827 Main IF/Audio Board should be studied along with the following:-

The input signal is passed via a 30MHz Input Low Pass Filter and a 3dB pad to a balanced RF amplifer 7TR5/6 (2 X BFW30). This amplifer has a flat response between 100kHz and 30MHz with additional negative feedback giving a gradual gain reduction down to 10kHz. The optional Preselector BP 2030 (where fitted) is switched in place of the 3dB pad when Wideband is deselected.

Differential transformer outputs 7T2/3 from 7TR5/6 drive a high level mixer 7IC3 (SL6440C). 'Up Conversion' provides an output at the 1st IF frequency of 46.205MHz which is filtered by 75ohm Roofing Filter 7FL1 at a bandwidth of 16kHz. The subsequent signal is applied to a double bridged 'T' attenuator 7D17-20 (4 X HP5082-3081) which provides up to 55dB of attenuation.

Attenuator control is performed by drawing current through i.e. turning 'ON' the shunt diodes 7D19,20 and turning 'OFF' the series diodes 7D17,18. This is performed by a voltage to current control circuit comprising 7IC4, 7TR8, 7TR9, 7IC5, 7TR10, 7TR11 which enables attenuator control over the range 0-4.5V. CMOS Op-Amp 7IC4 (CA3140E) has RF AGC voltage applied via time constant components 7R60, 7C91, 7R64. Transistor 7TR20 (BC547B) is used to 'quench' AGC voltage under remote control.

7TR12 (BFX89) provides gain and isolation between the attenuator and the second high level mixer 7IC6 (SL6440C). 'Down Conversion' provides an output at 1.4MHz where the signal is passed to the Main IF/Audio Board (BP1827).

Bias for both Mixer circuits 7IC3 and 7IC6 is controlled by 7TR7,13 (BC560B) providing 25mA bias current to each mixer. This condition is met when a 3V differential exists between 7TP7 and 7TP8 - adjusted by 7RV3. Both of the Mixer circuits form part of the synthesiser-see Section 4.2 Synthesiser and VCO circuit.

The Main IF/Audio Board BP1827 provides the main selectivity of the receiver. Selection of the three bandwidths is by BCD-Decimal decoder 10IC7 (74LS145) selecting a crystal filter for 3kHz and 8kHz positions while 16kHz employs a matching 3dB pad 10R14-16. Diodes 10D1,D4,D5 protect the decoder outputs from extraneous voltage produced by relays 10RLJ,K,L,M,N,P. Each selectivity position uses relays on input and output to provide maximum isolation from each other, only the pair of relays associated with the chosen selectivity position is energised-the remainder being open circuit. The 16kHz position is effectively the bandwidth of the Roofing Filter 7FL1 on the RF/IF Board. A 3dB pad matches the insertion loss of the other two selectivity positions and preserves the load impedance on the second high level mixer 7IC6. In order to ensure that this pad does not impair the response of the 8kHz and 3kHz selectivity positions, 10C21 (22pf) forms part of a capacitive attenuator with the O/C contact leakage capacity of 10RLN thus enhancing the isolation when this position is de-selected.

The 1.4MHz IF amplification is performed after the main selectivity. 10IC1,IC2 (MC1350P) and 10TR1 (BFR54) comprise a 90dB gain controlled amplifier some 80kHz wide. 10RV1 allows gain reduction matching between 10IC1 and 10IC2 under AGC conditions. 10TR1 is a high current high dynamic range buffer stage from where the signal is split off to the Product Detector, IF AGC Detector and IF Output stages.

Double balanced mixer 10IC13 (SL1641C) forms a product detector with 1405kHz from the Synthesiser Board to produce a 5kHz audio output for a 1.4MHz IF input. The audio signal is amplified and filtered by 10TR9 (BC547B), 10CH5 (10mH), 10C97,98 (5n6) and output via 10STC 2 to gain controls 11RV2 (600 ohm Line Audio) and 11RV3 (L.S. Audio).

IF AGC is derived from a fast acting AGC detector 10IC15 (SL623C). 10RV4 sets the point above which AGC output voltage is produced at 10IC15-4 (not to be confused with AGC threshold). The AGC voltage is split off to RF2 meter circuit via 10STC2 and to the AGC time constant selector switch 10IC6. AGC selection is by two control bits via 10STC1 AGC Mode LS Digit and AGC Mode MS Digit. These provide AGC modes as Table 4.1.

Table 4.1
AGC Selection

MSD	LSD	Function
0	0	None
0	1	Fast AGC (X1,Y1)
1	0	Manual Gain
1	1	Slow AGC

AGC voltage from 10D12 (BAX13) charges time constant capacitor 10C70 (10u) via 10R66 (15k). 10R63 (4M7) provides a discharge path for 10C70. This is the situation for SLOW AGC. FAST AGC enables transmission gate X1 Y1 10IC5 (MC14052B) connecting 10R175 (1k) in parallel with 10R66 and 10R176 (220k) in parallel with 10R63. This reduces the charge and discharge time of 10C70. 10TR18 (BC547B) and 10R172 'quench' the AGC line under remote control. Quad transmission gate 10IC5 (MC14016B) selects either AGC voltage from 10C70 or manual IF gain voltage from 10C71 and 10R65 under logic control as in Table 4.1. The remaining two gates in 10IC5 form a 2 input NOR gate with the MSD effectively inverted so that Manual IF gain is only enabled 10IC5-6 when the MSD is 1. 10IC4a (CA3240E) provides a low impedance for level shifting by 10IC3b (CA3240E) and summing of 'AGC threshold' voltage from 10RV2 (2k2) by 10IC3a. 'Half rail' reference voltage is applied to both amplifiers (10IC3a,b) and changes in its level will not be seen at the output. Variations in HT supply are not therefore superimposed on the AGC control voltage output from 10IC3a.

RF AGC is developed completely separate from the 1.4MHz IF amplifier and is connected at all times. Connected straight after the main selectivity a two stage wideband amplifier 10TR3,4 (BFR54) drives a fast acting AGC detector 10IC9 (SL1623C). RF AGC threshold is set by 10RV6 (1k) and the control voltage is routed to the RF & 1st IF Board via 10STC1.

IF output at 100kHz is provided by a mixer circuit using a 'high side' crystal oscillator to produce an 'erect' frequency characteristic. 10TR2 (BFR54) buffers the 1.4MHz IF output and provides a low impedance drive to double balanced mixer 10IC30 (SL1641C). A Colpitts oscillator is formed around Dual MOSFET 10TR15 (40673) and quartz crystal XTL1 (1500kHz). The resulting 100kHz output from 10IC30

is passed through a low pass filter 10C222-224,CH12,13 with a -3dB cut off of 185kHz. Tuned buffer 10TR16 (BC547B) limits the -3dB bandwidth to approx. 50kHz and allows output level adjustment (10RV11). PNP transistor 10TR7 (BC560B) provides impedance transformation and a 50ohm output at 100mV.

Two independently adjusted audio amplifiers are employed for line driving and external loudspeaker monitoring. Junction FET 10TR8 (UC734B) drives the audio amplifier circuit 10IC20 (TB810S) from a low impedance source, resulting in optimum low noise operating conditions for the latter. In order to maintain stability the bandwidth of 10IC20 is restricted by 10C141 (330p) and 10C140 (1n5). The output is coupled via 10C147 (100u) to centre tapped line isolating transformer 10T1, allowing matching of a 600 ohm line to some 4-8 ohms for the amplifier. The transformer drives but does not terminate a 600 ohm line. 10IC21a (CA3140E) acts as a half wave detector with 10D19 (BAX13) and with IC21b drives the 'line level' meter circuit via 10STC2. Operation of the external loudspeaker audio amplifier 10TR7 and 10IC22 is similar to the above. The output drives headphones via 10PL7 and 1SK5 and external loudspeaker via 10PL7 and 1SK3.

An open collector transistor 10TR9 (BC547B) switches 'ON' at and above 10.5MHz and is output via 10PL2 and 1SK3. Switching is under software control via 10STC1.

4.2 SYNTHESISER AND VCO CIRCUIT

The following should be read in conjunction with BP2023 1650/6 Receiver Synthesiser Circuits Block Diagram bound in Part 2. Refer to BP2021 1650/6 Chassis Interconnections & Misc. Modules for connections etc. between the modules described.

Table 4.2
Synthesiser Frequencies

Tuned Freq.	VCO Range	1st Loop	
0.010MHz	)	46.214MHz	
	) LF		
5.794MHz	)	51.998MHz	
	) LF+1		1st Oscillator is
12.794MHz	)	58.998MHz	46.204MHz above signal
	) HF-1		freq. in 2kHz steps.
20.794MHz	)	66.998MHz	
	) HF		
30MHz	)	76.204MHz	

2kHz step+	2nd Loop	Comparison Freq.	
0.005kHz	44.805,995MHz	5.995kHz	
			2nd Oscillator is
1.000kHz	44.805,000MHz	5.000kHz	1.4MHz below 1st IF
			in 5Hz steps
2.000kHz	44.804,000MHz	4.000kHz	

--oOo--

Example 4.1
19.999,995MHz Tune Frequency

19.999,995MHz Tune frequency is produced by 66.204,000MHz 1st oscillator & 44.804,005MHz 2nd oscillator.

Example 4.2
20.000,000MHz Tune Frequency

20.000,000MHz Tune frequency is produced by 66.204,000MHz 1st oscillator & 44.804,000MHz 2nd oscillator.

Example 4.3
20.000,005MHz Tune Frequency

20.000,005MHz Tune frequency is produced by 66.206,000MHz 1st oscillator & 44.805,995MHz 2nd oscillator.

Circuit diagrams BP1828 Synthesiser and VCO Board should be studied along with the following:-

The 1650/6 Synthesiser is a two phase locked loop design. The first loop generating frequencies covering the tuned frequency range 10kHz to 30MHz in 2kHz steps, the second loop providing 2kHz interpolation in 5Hz steps. Table 4.2 shows the operating frequencies of the two loops, their setting and interelation being under software control. Worked examples are shown for particular Tune Frequencies in Example 4.1 to Example 4.3.

8IC2 (SP8690B), 8IC3 (LF356N), 8IC4 (HEF4750), 8IC5 (HEF4751) and 9TR1 (40673) form a phase locked loop circuit. 8IC4 functions as a dual output phase comparator, Phase Comparator 1 (PC1) is a sample and hold circuit providing a very accurate control voltage. Phase Comparator 2 (PC2) is a wide range digital circuit with three states-positive, negative and high impedance. The output comprises a pulse train of varying mark/space ratio depending upon the phase difference between the reference (2kHz derived from the 5.6MHz standard) and the output of the Variable Ratio Divider 8IC5. Close to lock PC2 becomes high impedance and sample and hold comparator PC1 takes over. This technique gives rapid switching and very low reference frequency sidebands. PC1 and PC2 are summed into a low noise integrator circuit 8IC3. The integrator is 'half rail' biased so that digital comparator PC2 may provide both positive and negative correction i.e. $\pm$ 6V. 'Out of lock' indication is available at 8IC4-1.

The Variable Ratio Divider provides 2kHz output drive to the Phase Comparator. The divide ratio is set by 8D9-12 (BAX13), 8IC7 (MC14011B), 8IC8 (MC14504B) on a bit parallel digit serial basis. The Variable Ratio Divider controls the 'divide by 10/11' prescaler 8IC2 which is driven by VCO buffer 9TR3 (40673)

The Voltage Controlled Oscillator has four ranges, selected by relays 9RLA-D, in order to reduce the varicap diode control line sensitivity and the 'inband' phase noise. Separate buffered outputs are provided, 9TR2 (40673) for the 1st Signal Mixer and 9TR3 (40673) for the prescaler 8IC2.

The second phase locked loop generates frequencies in the range 44.804,000MHz to 44.805,995MHz in 5Hz steps which are applied to the second signal mixer.

8TR7 (BFX89), 8XTL1 (14935kHz) and 8D16 (MV1648) form a third overtone voltage controlled crystal oscillator (VCXO). 8TR6 (40673) amplifies and splits the oscillator signal, from the drain via 8PL9 to the 2nd signal mixer and from the source, tapped down by 8RV5 (220R), to IC26 (SL1641). Mixed with the eighth harmonic of 5.6MHz it produces an output in the range 4kHz to 5.995kHz. 8IC28 (MC14001B) acts as an amplifier/limiter to produce a 15V p-p squarewave to feed phase comparator A input of 8IC27 (MC14046B). 8IC31 (MC14526B) and 8IC32 (MC14569B) form a variable ratio divider preset by two eight stage shift registers 8IC33,34 (MC14094B). The output from the variable ratio divider is in the range 4kHz to 5.995kHz and is fed to phase comparator B input 8IC27 via 8IC28 (MC14001B). 8IC25 (CA3240E) amplifies the phase comparator error voltage produced and applies it to varicap diode 8D16 (MV1648). Altering the variable ratio divider under software control pulls the VCXO over it's 2kHz range. 'Out of lock' detection is provided by 8IC29, 8D17 (BAX13), 8R73 (100k) and 8C110 (10n). The output at collector 8TR9 (BC547B) is 'ORed' with the first phase locked loop 'out of lock' detector at 8STC1-1 where it's state may be read by the micro-computer.

The 5.6MHz standard is 8OSC1, a voltage controlled ovened crystal oscillator. Trimming is via 8RV2 (1k) and the signal is shaped and distributed to the two phase locked loops via 8IC15 (74LS04).

A Colpitts oscillator is formed around Dual MOSFET 8TR20 (40673) and quartz crystal 8XTL2 (1405kHz). The output drives product detector 10IC13 via 8RV3 (1k) and 8PL7.

4.3 CONTROL, DISPLAY AND MICROCOMPUTER CIRCUITS

The following should be read in conjunction with BP2042 1650/6 Receiver ,Control and MCU Circuit, Block Diagram BP2025 1650/6 Interface board, BP1975 1650/6 Front Panel Display and BP2043 1650/6 Micro-Computer board bound in Part 2. A simplified program executive flowchart BP2024 should also be studied.

The micro-computer unit uses a MC6802P microprocessor (MPU 13IC2), 8K bytes of 'read only memory' (ROM-2 X 2732, 13IC8,9), 2K bytes of 'random access memory' (RAM-6116LP4, 13IC5), and triple timer 13IC1 (MC6840P). Eight external peripherals may be accessed by the system. All of the RAM is non-volatile, it's power being supplied by a 3.6V 100mAH battery when the receiver is 'off'. Circuitry is incorporated in order to prevent memory corruption at power down during a 'write' to RAM. 13IC7-4,5,6-8,9,10 (MC14011B) form an RS bistable. At power down the RS bistable changes state because current is no longer supplied to Opto-Isolator 13IC15 (MCT2), in doing so the 'chip select' pulse to 13IC5 (6116LP4) is inhibited. If, however, a power down occurs during a 'write ' period this is completed as 13IC7-4 cannot change state when it is Low (0). The RAM is therefore never deselected during a 'write' period. Threshold comparator 13IC6 (CA3140E) detects the supply falling to approx. 8.3V (from 10V) and disables Opto-isolator 13IC15. 0.5V hysteresis is incorporated around the switch over point to prevent mis-triggering. 13IC4 (MC14528B) forms a monostable with 13R16 (100k) and 13C13 (10u) which generates a reset pulse (100-200mS) at power up and from 13IC5-4 going momentarily Low (0). This reset pulse is coupled to 13IC2 via 13TR1 (BC547B) allowing the MPU reset vectors to be loaded.

All Data lines and Address lines A0-A11 are 'pulled up' by 13R2 (47k) and 13R20 (47k) in order to provide known states during power down. Partial decoding is used by the MPU to address both on and off board peripherals. The repeats that occur are not accessed by the software.

It is important that data remains static on the data bus D0-D7 (13IC12-27-33)for at least 30nS after the Enable line (13IC12-37) goes Low (0). In order to improve the margin of safety all peripherals are enabled via leading edge triggered monostable 13IC11 (74LS123). The resulting 'output enable' is shorter, approx. 450nS as opposed to the 'input enable' of 610nS. This gives a much greater margin of safety i.e.610-450=160nS before the 'input enable' falls but with the data lines being static until at least

that time. The actual monostable time is not critical to the system operation. The delay provided removes any possible race hazard between Enable and Data caused by 'clock skewing'.

The micro-computer sends and receives mainly serial data signals to and from the receiver via the interface board BP2025. The LED front panel display is controlled by 12IC10 (74LS74) and data is converted to latched parallel form by display drivers 11IC4,5,6,7 (2 X MM5450). Data is latched into the display driver after 35 serial data bits have been sent. The LED front panel display is fully static in operation. 12IC10 also passes the receiver's remote control output and reverted data signal to the rear panel connector 1PL1. The synthesiser (see Sect 4.2 Synthesiser and VCO circuit) is controlled via 12IC9 (74LS374). Signal and receiver function settings are also controlled by 12IC9 in conjunction with the latched parallel data converter 12IC2,3,4 (3 X MC14094B). Various sense and remote control inputs are passed to the micro-computer via 12IC7,8 (2 X MC14503B).

All the front panel keys, with the exception of 'STANDBY' are organised as a six by six matrix. In order to reduce radiated interference, this matrix is only 'actively' scanned on demand. Key board 'write' signals from 12IC12 (74LS374) go to the six keyboard matrix rows. The six keyboard matrix columns are 'read' by 12IC11 (MC14503B) and 'pulled up' by 12R11 (2k2). Normally all the rows are held Low (0) and, with no key pressed, all the columns are High (1). The keyboard is read in this fashion every 50mS. A key press causes one of the columns to go Low (0) and this initiates a scan routine by the micro-computer. Each row in turn D0-D5 (12IC11) is taken Low (0) and the corresponding column is identified by 12IC11. A consecutive scan, 50mS later, will cause the micro-computer to act on the key press, however any change will cause the key press to be ignored and a return to the normal reading routine.

The tuning knob, used for test purposes only, provides two inputs to the micro-computer triple timer 13IC1 (MC6840P) via 11IC1 (MC14583B), 11IC2 (MC14077B) and 11IC3 (MC14506B). These circuits convert the two-phase pulse stream from the turned knob into separate 'Up' (knob turning clockwise) and 'Down' (knob turning anti-clockwise) pulse streams which can be separately counted and accumulated by the micro-computer.